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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,668	09/23/2003	Chie Fukuda	50212-539	9103

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EXAMINER

CHIEM, DINH D

ART UNIT PAPER NUMBER

2883

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/667,668

Applicant(s)

FUKUDA ET AL.

Examiner

Erin D. Chiem

Art Unit

2883

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 05 July 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-8, 14-23 and 29 is/are pending in the application.
- 4a) Of the above claim(s) 9-13 and 24-28 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-8, 14-23, and 29 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election without traverse of Invention I and Species A and Species C, drawn to claims 1-8, 14-23, and 29 in the reply filed on July 5, 2005 is acknowledged. There is no declaration whether the election is with or without traverse nor is there any argument found in Applicant's election, therefore, the election will be treated as an election without traverse and the restriction is made FINAL.

### ***Drawings***

2. The drawings are objected to under 37 CFR 1.83(a) because they fail to show the "outer periphery side" shift of the light emission layer and the "outer periphery side" of the waveguide as described in the specification. Furthermore, element 204 is not shown in the Figures. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets

Art Unit: 2883

may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

3. Claims 2 and 17 are objected to because of the following informalities: the recitation describing the placement of the light emission layer with respect to the optical semiconductor element of "an outer periphery side" is unclear. The Specification only broadly mentioned the "outer periphery" in the Summary of Invention section and the Specification does not provide enough clarification in the Detail Description. For the purpose of examination this limitation, being relative to no reference point nor a discreet distance, shall be ignored.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 2, 7, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koren et al. (US 5,127,081) in view of Krishnamoorthy.

Art Unit: 2883

Koren teaches an integrated optical comprising an optical semiconductor element 310 (Fig. 4) including a light emission layer 330 and outputting light of a predetermined wavelength, an optical circuit element including a silicon substrate 365, and optical waveguide 340 in which the light from said optical semiconductor element propagates and which is provided on said substrate. Furthermore, Koren took official notice that it is well known to those skilled in the art to form anti-reflective coating on the transmitting end of the optical amplifier to increase transmission efficiency and Koren further teaches integrating gratings onto the waveguide in order to provide distributed feedback, which has long been taught by Liou et al. (col. 6, lines 4-13).

However, Koren does not teach bonding the optical circuit element to the surface of the silicon substrate.

Krishnamoorthy (US 6,504,977 B1) teaches flip-chip bonding the circuit on to the substrate 300 (Fig. 3). for the purpose of reducing inductance power distribution to the integrated circuit.

Since Koren and Krishnamoorthy are both from the same field of endeavor, the purpose disclosed by Krishnamoorthy would have been recognized in the pertinent art of Koren.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to employ flip-chip bonding to a optical circuit onto a silicon substrate such as one taught by Koren. **The motivation** for using flip-chip bonding technology is its ability to reduce inductance power distribution to the integrated circuit.

Art Unit: 2883

Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koren and Krishnamoorthy as applied to claim 1 above, and further in view of Okada et al. (US 6,435,734 B2).

Koren and Krishnamoorthy teach an integrated optical element including a light emission layer, an optical waveguide formed on the silicon substrate, having grating and anti-reflective coating to increase transmission efficiency, and wherein the optical circuit is flip-chip bonded to reduce inductance power distribution to the integrated circuit.

However, Koren and Krishnamoorthy do not teach the space between the optical semiconductor element facing the optical waveguide is filled with resin having a refractive index of 1.300 or more but 1.444 or less.

Okada teaches an optoelectronic module using a silicone-type resin having refractive index  $n=1.4$  (col. 3, line 26) for the purpose of reducing reflection loss.

Since Koren, Krishnamoorthy, and Okada are both from the same field of endeavor, the purpose disclosed by Okada would have been recognized in the pertinent art of Koren and Krishnamoorthy.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to select a resin having refractive index which matches the refractive index of the waveguide to contain the light beam within the resin medium and transmit from the optical element such as the amplifier taught by Krishnamoorthy to the waveguide **The motivation** for filling the space with waveguide refractive index matching resin is to reduced reflection loss.

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koren and Krishnamoorthy as applied to claim 1 above, and further in view of Forrest et al. (US 2002/0031297 A1).

Koren and Krishnamoorthy teach an integrated optical element including a light emission layer, an optical waveguide form on the silicon substrate, having grating and anti-reflective coating to increase transmission efficiency, and wherein the optical circuit is flip-chip bonded to reduce inductance power distribution to the integrated circuit.

However, Koren and Krishnamoorthy together do not teach the optical circuit tilts at an angle of 3 to 8 degrees.

Forrest teaches the laser to tilt at an angle of 7 degrees transmitting toward the optical amplifier for the purpose of preventing optical feedback into the optical amplifier.

Since Koren, Krishnamoorthy, and Okada are both from the same field of endeavor, the purpose disclosed by Okada would have been recognized in the pertinent art of Koren and Krishnamoorthy.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to employ this range of angle tilt given what Forrest has taught for the purpose of preventing optical feedback even though the component taught by Forrest was a laser and not an optical circuit. One of ordinary skills in the art would recognize that regardless of what optical element is use, the criticality of Forrest's teaching is in the coupling of the optical signal relative to the optical axis. **The motivation** for tilting at an angle between 3 and 8 degrees is for the purpose of preventing optical feedback into the optical amplifier.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koren and Krishnamoorthy as applied to claim 1 above, and further in view of Chandrasekhar et al. (US 6,411,764 B1)

Koren and Krishnamoorthy teach an integrated optical element including a light emission layer, an optical waveguide formed on the silicon substrate, having grating and anti-reflective coating to increase transmission efficiency, and wherein the optical circuit is flip-chip bonded to reduce inductance power distribution to the integrated circuit. Furthermore, Koren and Krishnamoorthy teaches the refractive index of the cladding must be less than the refractive index of the core, thus reads upon the limitation of having a relative refractive index difference between a core and a cladding of said optical waveguide in the optical circuit element is 1.0% or more.

However, Koren and Krishnamoorthy does not disclose a spot size conversion structure whose FFP is 15 degrees or less

Chandrasekhar teaches a core spot size converter having a far field angle approximately 6 degrees for the purpose of efficiently coupling the signal from the waveguide core to the photodetector (col. 5, line 6).

Since Koren and Krishnamoorthy and Chandrasekhar are all from the same field of endeavor, the purpose disclosed by Chandrasekhar would have been recognized in the pertinent art of Koren and Krishnamoorthy.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to perform mode matching by epitaxially form the waveguide to the correctness. If the thickness of the waveguide increases, the size of the mode decreases thereby



Art Unit: 2883

the mode is compressed and the mode size becomes smaller and a more of the energy is confined within the waveguide. **The motivation** for forming a waveguide having the predetermined thickness such that the far field angle is 15 degrees or less is for evanescent coupling wherein mode matching is critical to the efficiency (col. 4, lines 30-67).

Regarding claims 14-23 and 29, the 103 rejections above applied to all of the limitations except for the limitation of having N (integer of 2 or more) number optical semiconductor elements and N number of waveguides, and N number gratings.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to epitaxially grow multiple semiconductor layers and etch away the material leaving the array of semiconductor elements and waveguides and gratings, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

### ***Conclusion***

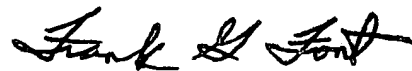
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erin D. Chiem whose telephone number is (571) 272-3102. The examiner can normally be reached on Monday - Thursday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank G. Font can be reached on (571) 272-2415. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2883

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art Unit 2883



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